CLAIMS

What we claim is:

[c1] 1. A data communications system including a bidirectional buffer coupled among a transmitter, a receiver, and a transmission line, wherein the bidirectional buffer comprises:

an input amplifier section that generates differential data signal pairs from a difference between differential transmission line signals and differential transmitter signals; and

an output differential amplifier section that generates output logic signals from the differential data signal pairs, wherein the output logic signals represent data received on the transmission line, wherein input noise at the input amplifier section is suppressed using an asymmetric transfer characteristic that offsets output signal logic levels with regard to the input noise.

[c2] 2. The data communications system of claim 1, wherein the asymmetric transfer characteristic is skewed using an asymmetrical transistor configuration at an output side of a differential pair that forms the output differential amplifier section, wherein the input noise introduced by a floating input is suppressed.

[c3] 3. The data communications system of claim 1, wherein a first differential amplifier of the input amplifier section generates positive polarity data signals from a difference between a positive polarity transmission line signal and a positive polarity transmitter signal, wherein a second differential amplifier of the input amplifier section generates negative polarity data signals from a difference between a negative polarity transmission line signal and a negative polarity transmitter signal, wherein common mode rejection is independently controlled in

each of the first and second differential amplifiers using bias signals generated in response to an output common mode feedback voltage from the first and second differential amplifiers.

[c4] 4. A bidirectional bridge circuit for interfacing between a transmission line and a communication device, the bidirectional bridge circuit comprising:

an input amplifier circuit including a differential coupling to the transmission line and a differential coupling to the communication device, wherein the input amplifier circuit includes a first and a second differential amplifier, wherein the input amplifier circuit generates a positive polarity difference signal and a negative polarity difference signal from differential signals of the transmission line and the communication device;

wherein the first differential amplifier is coupled to amplify the positive polarity difference signal and generate a positive polarity data signal, wherein the second differential amplifier is coupled to amplify the negative polarity difference signal and generate a negative polarity data signal; and

an output differential amplifier coupled to receive the positive polarity data signal and the negative polarity data signal and generate an output logic signal representative of data received via the transmission line, wherein the output differential amplifier suppresses input noise using an asymmetric transfer characteristic that offsets output signal logic levels with regard to input noise.

[c5] 5. The bridge circuit of claim 4, wherein the output differential amplifier suppresses noise introduced by a floating input using the asymmetric transfer characteristic, wherein the output differential amplifier transfer characteristic is skewed using an asymmetrical transistor configuration at an output side of a differential pair that forms the output differential amplifier.

[c6] 6. The bridge circuit of claim 4, wherein common mode rejection is independently controlled in each of the first and second differential amplifiers using bias signals generated in response to an output common mode feedback voltage from the first and second differential amplifiers.

[c7] 7. The bridge circuit of claim 4, wherein the first differential amplifier includes common mode feedback circuitry controlled by the output common mode of the first differential amplifier to generate a feedback voltage that suppresses a common mode gain of the first differential amplifier, wherein the common mode rejection of the first differential amplifier is increased.

[c8] 8. The bridge circuit of claim 4, wherein the second differential amplifier includes common mode feedback circuitry controlled by the output common mode of the second differential amplifier to generate a feedback voltage that suppresses the common mode gain of the second differential amplifier, wherein the common mode rejection of the first differential amplifier is increased.

[c9] 9. An amplifier comprising:

a differential amplifier pair coupled to receive positive polarity data signals and negative polarity data signals generated from each of a transmission line differential signal pair and a transmitter differential signal pair; and

output circuitry coupled to the differential amplifier pair, wherein the output circuitry produces an output logic signal in response to the positive polarity data signals and the negative polarity data signals, wherein the output logic signal represents data received on the transmission line, wherein electronic noise is suppressed using an asymmetric transfer characteristic that offsets output signal logic levels with regard to input noise signals.

[c10] 10. The amplifier of claim 9, wherein the asymmetric transfer characteristic is generated by skewing a transfer characteristic of the differential amplifier pair using an asymmetrical transistor configuration at an output side of the differential amplifier pair.

[c11] 11. The amplifier of claim 9, wherein symmetry is controlled in switching transients of the output logic signal using at least one logic gate having a threshold voltage that is higher than a mid-supply voltage of the output circuitry.

[c12] 12. The amplifier of claim 9, wherein the output circuitry comprises at least one NAND logic gate with a diode-connected n-type metal-oxide-semiconductor field-effect transistor (MOSFET) in a ground path, wherein a logic threshold voltage of the NAND logic gate is higher than a mid-supply voltage while switching rise and fall times are maintained as approximately symmetric.

[c13] 13. A method of suppressing differential input signal noise in output logic signals, comprising:

receiving differential data signals of opposite polarity from a transmission line and a transmitter at a differential amplifier;

skewing an output transfer characteristic of the differential amplifier, wherein the asymmetric transfer characteristic offsets output signal logic levels with regard to input noise signal levels;

generating output logic signals representative of data received via the transmission line using the asymmetric transfer characteristic; and

coupling the output logic signals to a receiver.

[c14] 14. A method for providing a bidirectional communications interface including a bridge connecting a transmitter and a receiver to a transmission line, the method comprising:

generating positive and negative polarity data signals using separate differential amplifiers that receive differential signal pairs from each side of a differential link to the transmission line and the transmitter;

generating output logic signals representing data received on the transmission line using the positive polarity data signals and the negative polarity data signals;

suppressing effects of input noise on the output logic signals by skewing an output amplifier transfer characteristic; and

providing the output logic signals to the receiver.

[c15] 15. The method of claim 14, further comprising independently controlling common mode rejection in each of the separate differential amplifiers using bias signals generated in response to an output common mode feedback voltage from each of the differential amplifiers

[c16] 16. The method of claim 14, further comprising independently controlling common mode rejection in each of the separate differential amplifiers, wherein controlling common mode rejection comprises:

receiving a common mode output voltage from a differential amplifier;

generating a common mode feedback voltage using the common mode output voltage; and

suppressing a common mode gain of the differential amplifier in response to the common mode feedback voltage, wherein the common mode rejection of the differential amplifier is increased.

[c17] 17. The method of claim 14, further comprising controlling symmetry in switching transients of the output logic signals by increasing a logic threshold

voltage of a logic gate of the output amplifier above a mid-supply voltage of the logic gate.

[c18] 18. A bidirectional communications system comprising:

at least one transmitter;

at least one receiver; and

at least one buffer coupling the at least one transmitter and the at least one receiver to at least one transmission line, the at least one buffer comprising:

input amplifier circuitry coupled to receive transmission line differential signals and transmitter differential signals and generate data signals of opposite polarities by subtracting the transmitter differential signals from the transmission line differential signals of corresponding polarity; and

output circuitry that amplifies and combines the generated data signals to provide single-ended logic signals representative of data received on the transmission line, wherein the logic signals are coupled to the receiver, wherein the output circuitry suppresses input noise using an asymmetric transfer characteristic that offsets output signal logic levels with regard to input noise.

[c19] 19. At least one semiconductor chip having a bidirectional bridge connecting each of a transmitter and a receiver to a transmission line, wherein the bidirectional bridge includes an output amplifier comprising:

means for receiving differential data signals of opposite polarity from a transmission line and a transmitter at a differential amplifier;

means for skewing an output transfer characteristic of the differential amplifier, wherein the asymmetric transfer characteristic offsets output signal logic levels with regard to input noise signal levels;

means for generating output logic signals representative of data received via the transmission line using the asymmetric transfer characteristic; and

means for coupling the output logic signals to a receiver.

[c20] 20. A computer readable medium including executable instructions which, when executed in a processing system, provide a bidirectional communications interface including a bridge connecting a transmitter and a receiver to a transmission line by:

generating positive and negative polarity data signals using separate differential amplifiers that receive differential signal pairs from each side of a differential link to the transmission line and the transmitter;

generating output logic signals representing data received on the transmission line using the positive polarity data signals and the negative polarity data signals;

suppressing effects of input noise on the output logic signals by skewing an output amplifier transfer characteristic; and

providing the output logic signals to the receiver.

[c21] 21. A bidirectional communication link, comprising:

means for receiving transmission line differential signal pairs and transmitter differential signal pairs;

means for generating differential data signals from a difference between differential transmission line signals and differential transmitter signals having a same polarity;

means for generating a single-ended output logic signal from the differential data signals, wherein the output logic signal represents data received in the transmission line differential signal pairs;

means for suppressing effects of input noise on the output logic signal by skewing an output amplifier transfer characteristic; and

means for coupling the output logic signal to a receiver.